REMARKS

In response to the Office Action mailed November 2, 2006, Applicants respectfully request entry of this amendment. Claims 1-30 were previously pending in this application. By this amendment, Applicants are canceling claim 2 without prejudice or disclaimer. Claims 1, 13, 24-26 and 30 have been amended. As a result, claims 1 and 3-30 are pending for examination with claims 1, 24, 26 and 30 being independent. No new matter has been added.

Rejections Under 35 U.S.C. §102

The Office Action rejected claims 1, 3-9, and 13-25 under 35 U.S.C. 102(b) as allegedly being anticipated by Lewis et al., US Patent 5,797,043 (hereinafter Lewis). Applicants respectfully disagree.

Claim 1, as amended, recites

> A processing system for accessing data, the processing system comprising:
> a processor for executing instructions;
> *a stream register unit being part of the processor* and configured to supply a first type of data to the processor, the first type of data being data supplied from a peripheral, *the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral*;
> a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register unit by a communication path, along which *said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO*; and
> a memory bus, *separate from the communication path*, connected between a data memory and the processor, across which the processor can access a second type of data, the second type of data being randomly accessible data held in the data memory.
> (Emphasis added).

As explained in Applicants' response to the Office Action mailed April 6, 2006, which is incorporated herein by reference, Lewis neither discloses nor suggests a processing system for accessing data, the processing system comprising: ... a stream register unit being part of the processor and configured to supply a first type of data to the processor, the first type of data being data supplied from a peripheral, the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral; a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register

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unit by a communication path, along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO; and a memory bus, separate from the communication path, connected between a data memory and the processor, across which the processor can access a second type of data, the second type of data being randomly accessible data held in the data memory, as recited in claim 1.

In view of the foregoing, claim 1 patentably distinguishes over Lewis.

Claims 3-23 depend from claim 1 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 1 and 3-23 is respectfully requested.

Claim 24, as amended, recites

A streaming data handling system, comprising:
a processor;
a stream register being part of the processor and configured to supply data from a peripheral to the processor, *the stream register including at least one stream register FIFO configured to store the data received from the peripheral*; and
a FIFO memory coupled to the peripheral to receive the data from the peripheral and connected to the least one stream register FIFO via a communication path,
wherein the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order.
(Emphasis added).

Lewis neither discloses nor suggests a streaming data handling system, comprising: ... a stream register being part of the processor and configured to supply data from a peripheral to the processor, the stream register including at least one stream register FIFO configured to store the data received from the peripheral; and a FIFO memory coupled to the peripheral to receive the data from the peripheral and connected to the least one stream register FIFO via a communication path, wherein the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order, as recited in claim 24.

In view of the foregoing, claim 24 patentably distinguishes over Lewis.

Claim 25 depends from claim 24 and is allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 24 and 25 is respectfully requested.

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Rejections Under 35 U.S.C. §103

The Office Action rejected claims 26-30 under 35 U.S.C. 103(a) as allegedly being unpatentable over Lewis et al., US Patent 5,797,043 (hereinafter Lewis), in view of Garcia et al., US Patent 6,433,785 (hereinafter Garcia). Applicants respectfully disagree.

Claim 26, as amended, recites

A stream register connectable between a processor and a peripheral, *the stream register being part of the processor* and comprising:
a receiver arranged to receive a request for a data item from the processor;
at least one FIFO configured to store the data item received from the peripheral; and
a stream engine, arranged to:
receive the request for the data item;
determine whether the requested data item is in the at least one FIFO;
if the requested data item is not in the at least one FIFO, send a stall signal to the processor; and
send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, if the data item is available, send the data item to the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the processor causing the processor to interrupt such that it can execute tasks other than the request.
(Emphasis added).

As discussed above, Lewis neither discloses nor suggests a stream register connectable between a processor and a peripheral, the stream register being part of the processor and comprising: ... a stream engine, arranged to: receive the request for the data item; determine whether the requested data item is in the at least one FIFO; if the requested data item is not in the at least one FIFO, send a stall signal to the processor; and send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, if the data item is available, send the data item to the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the processor causing the processor to interrupt such that it can execute tasks other than the request, as recited in claim 26.

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Furthermore, Garcia neither discloses nor suggests a stream register connectable between a processor and a peripheral, the stream register being part of the processor and comprising: … a stream engine, arranged to: receive the request for the data item; determine whether the requested data item is in the at least one FIFO; if the requested data item is not in the at least one FIFO, send a stall signal to the processor; and send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, if the data item is available, send the data item to the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the processor causing the processor to interrupt such that it can execute tasks other than the request, as recited in claim 26.

Therefore, neither Lewis nor Garcia teaches or suggests the limitations of claim 26.

In view of the foregoing, claim 26 distinguishes over the cited references and is in condition for allowance.

Claims 27-29 depend from claim 26 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 26-29 is respectfully requested.

<u>Claim 30</u>, as amended, recites

> *A stream register, being part of a processor*, connectable between the processor and a memory, the stream register comprising:
> a receiver arranged to receive a request for a data item from the processor;
> at least one FIFO configured to store the data item received from the peripheral; and
> *a stream engine, arranged to:*
> > *receive the request for the data item;*
> > *determine whether the requested data item is in the at least one FIFO;*
> > *if the requested data item is not in the at least one FIFO, send a stall signal to the processor; and*
> > *send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, if the data item is available, send the data item to the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the processor causing the processor to interrupt such that it can execute tasks other than the request.*
> (Emphasis added).

As discussed above, neither Lewis nor Garcia discloses or suggests a stream register, being part of a processor, connectable between the processor and a memory, the stream register comprising: ... a stream engine, arranged to: receive the request for the data item; determine whether the requested data item is in the at least one FIFO; if the requested data item is not in the at least one FIFO, send a stall signal to the processor; and send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, if the data item is available, send the data item to the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the processor causing the processor to interrupt such that it can execute tasks other than the request, as recited in claim 30.

Therefore, neither Lewis nor Garcia teaches or suggests the limitations of claim 30.

In view of the foregoing, claim 30 distinguishes over the cited references and is in condition for allowance.

Accordingly, withdrawal of the rejection of claim 30 is respectfully requested.
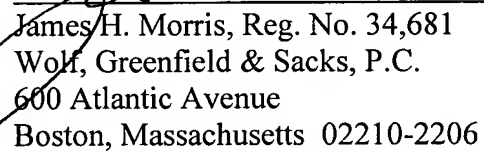
CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: March 2, 2007

Respectfully submitted,

By: _____

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